

In the Specification:

Please insert the following paragraph between paragraphs [0028] and [0029]:

Figs. 3E-3G are schematic diagrams that illustrate an apparatus for thermally coupling a semiconductor chip to a heat conducting device according to another exemplary embodiment of the invention.

Please amend paragraph [0059] as follows:

Relieving the stress in the direction perpendicular to the fins requires either compression or flow of the compliant thermally conductive material between the fins. In other exemplary embodiments of the invention, the microfin thermal joints depicted in Figs. 2 and 3 can be modified to enable the compliant material to flow more easily from one side of a microfin to the other side providing even more stress relief. For instance, the microfins need not be continuous but can have breaks/gaps along their length. The density of these gaps or breaks can be adjusted to correspond to the amount of flow expected. For example, relatively more gaps/breaks can be provided in the thermal microfins that are near the edges of the chip as compared to the center, since the relative displacement due to the difference in thermal expansion is larger near the edges. This can be illustrated with reference to the schematic diagrams of Figs. 3E, 3F and 3G, which illustrate an apparatus for thermally coupling a semiconductor chip to a heat conducting device according to another exemplary embodiment of the invention. In particular, Figs. 3E, 3F and 3G are schematic top plan views taken along slices through the middle of the different regions R1, R2 and R3 of the thermal joint (23) illustrated in Figs. 3B, 3C and 3D, respectively. As shown in FIGs. 3E~3G, the parallel interdigitated thermal microfins (21a, 22a) in the respective regions (R1, R2 and R3) of the thermal joint (23) are formed having respective gaps/breaks (g1, g2, and g3) along the lengths thereof. The density of the gaps (g1, g2 and g3) formed along the thermal microfins (21a, 22a) in respective regions (R1, R2 and R3) is shown to increase from the center region of the semiconductor chip toward the edge regions of the semiconductor chip.